THAT WHICH IS CLAIMED IS:

1. An asynchronous frame receiver comprising:

an input for receiving an asynchronous frame comprising a break character, the break character comprising a plurality of bits having a same value; and

a hot-plugging circuit for connecting to an asynchronous data bus that is operating, said hot-plugging circuit detecting the break character, and leaving an initial idle state and switching to at least one operating mode when the break character has been detected.

2. An asynchronous frame receiver according to Claim 1, wherein the asynchronous frame further comprises a synchronization character after the break character, the asynchronous frame receiver further comprising:

a clock recovery circuit that is activated after receiving the synchronization character at the input after detecting the break character.

3. An asynchronous frame receiver according to Claim 2, wherein said clock recovery circuit measures a clock period in the synchronization character.

4. An asynchronous frame receiver according to Claim 3, wherein said clock recovery circuit measures a clock period from a first falling edge after the break character to a last falling edge of the synchronization character.

5. An asynchronous frame receiver according to Claim 1, wherein said hot-plugging circuit comprises a state machine.

6. An asynchronous frame receiver according to Claim 1, further comprising a substrate; and wherein said hot-plugging circuit is on said substrate so that the asynchronous frame receiver comprises an integrated circuit.

7. A microcontroller comprising:

a universal asynchronous frame receiver transceiver (UART) comprising

an input for receiving an asynchronous frame comprising a break character, the break character comprising a plurality of bits having a same value; and

a hot-plugging circuit for connecting to an asynchronous data bus that is operating, said hot-plugging circuit detecting the break character, and leaving an initial idle state and switching to at least one operating mode when the break character has been detected; and

a processor connected to said asynchronous frame receiver.

8. A microcontroller according to Claim 7, further comprising a memory connected to said processor.

9. A microcontroller according to Claim 7, wherein the asynchronous frame further comprises a synchronization character after the break character, said UART further comprising:

a clock recovery circuit that is activated after receiving the synchronization character at the input after detecting the break character.

10. A microcontroller according to Claim 9, wherein said clock recovery circuit measures a clock period in the synchronization character.

11. A microcontroller according to Claim 10, wherein said clock recovery circuit measures a clock period from a first falling edge after the break character to a last falling edge of the synchronization character.

12. A microcontroller according to Claim 7, wherein said hot-plugging circuit comprises a state machine.

13. A method for connecting an asynchronous frame receiver to an asynchronous data bus that is operating, the method comprising:

setting the asynchronous frame receiver to an initial idle state;

receiving at an input of the asynchronous frame receiver an asynchronous frame comprising a break character, the break character comprising a plurality of bits having a same value; and

detecting the break character and switching the asynchronous frame receiver from the initial idle state to at least one operating mode.

14. A method according to Claim 13, wherein the at least one operating mode comprises a read mode.

15. A method according to Claim 13, wherein the asynchronous frame further comprises a synchronization character after the break character; and further comprising activating a clock recovery circuit after receiving the synchronization character at the input after detecting the break character.

16. A method according to Claim 15, wherein the clock recovery circuit measures a clock period in the synchronization character.

17. A method according to Claim 16, wherein the clock recovery circuit measures a clock period from a first falling edge after the break character to a last falling edge of the synchronization character.